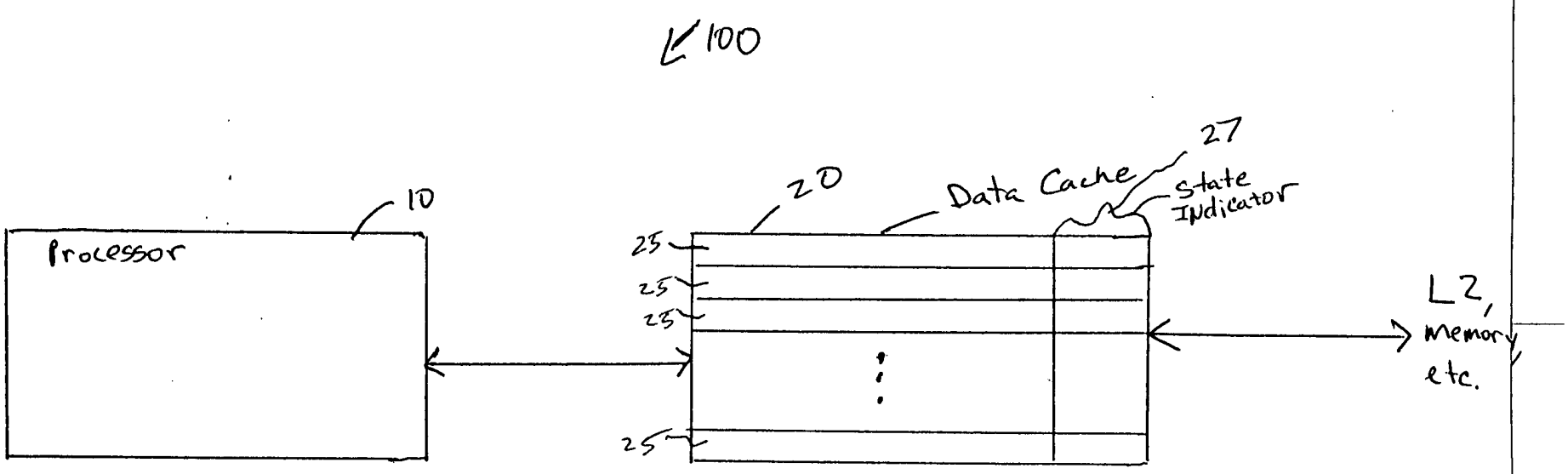
100
Processor
10
20
Data Cache
27
State Indicator
25
25
25
25
L2, memory etc.

Figure 1

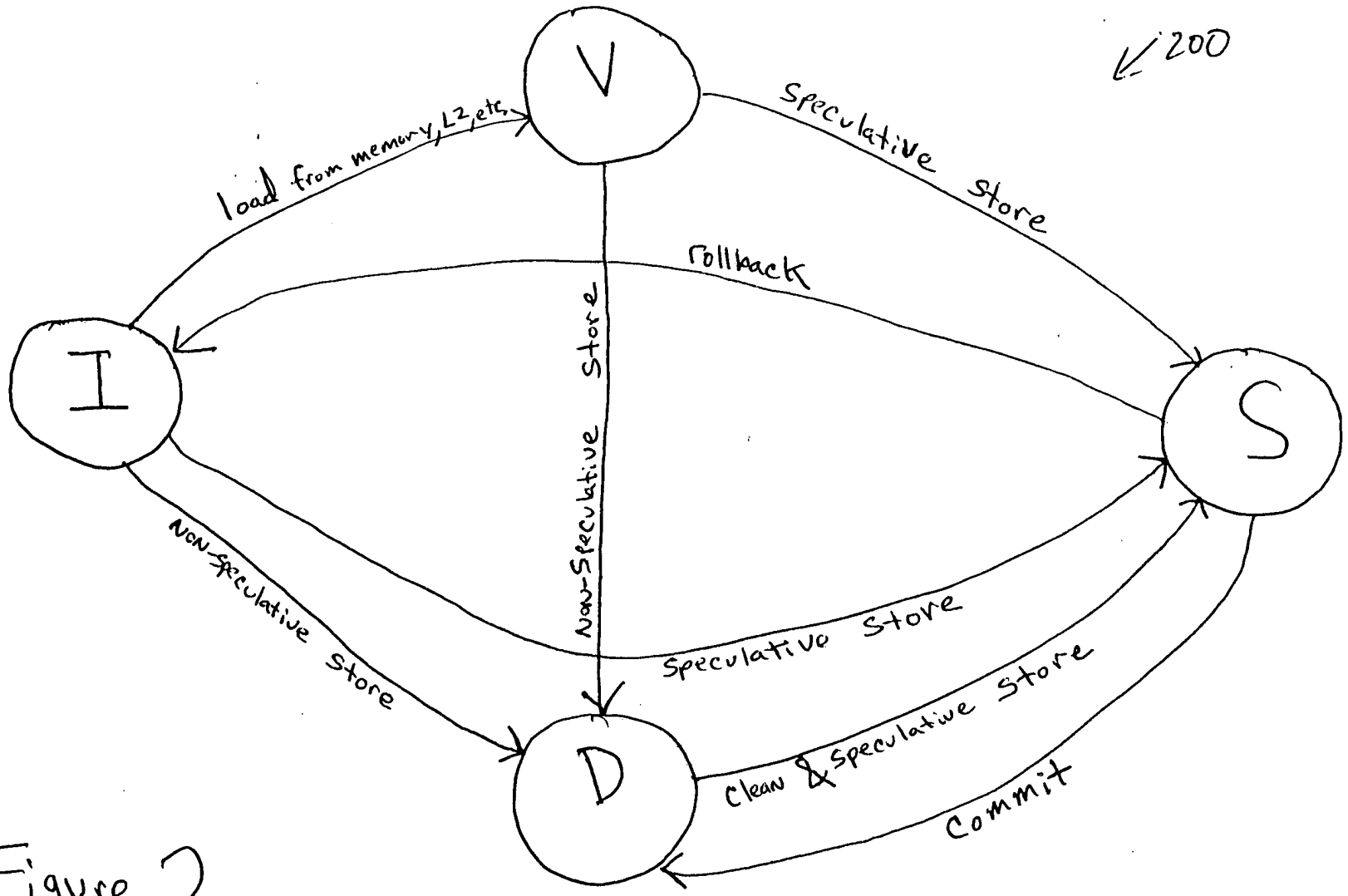
200
V
I
S
D
load from memory, L2, etc.
Speculative Store
Rollback
Non-Speculative Store
Non-Speculative Store
Speculative Store
Clean & Speculative Store
Commit

Figure 2

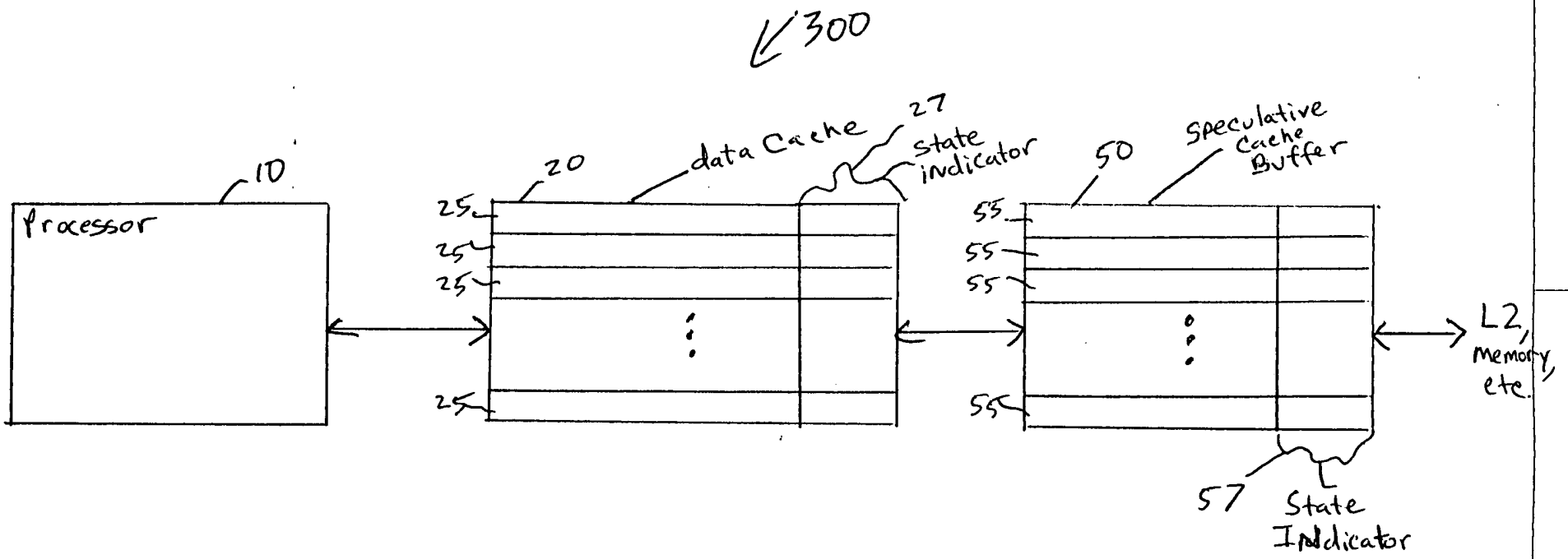
300
Processor
10
20
data Cache
27
state indicator
25
25
25
25
50
Speculative Cache Buffer
55
55
55
55
L2, memory, etc.
57
State Indicator

Figure 3

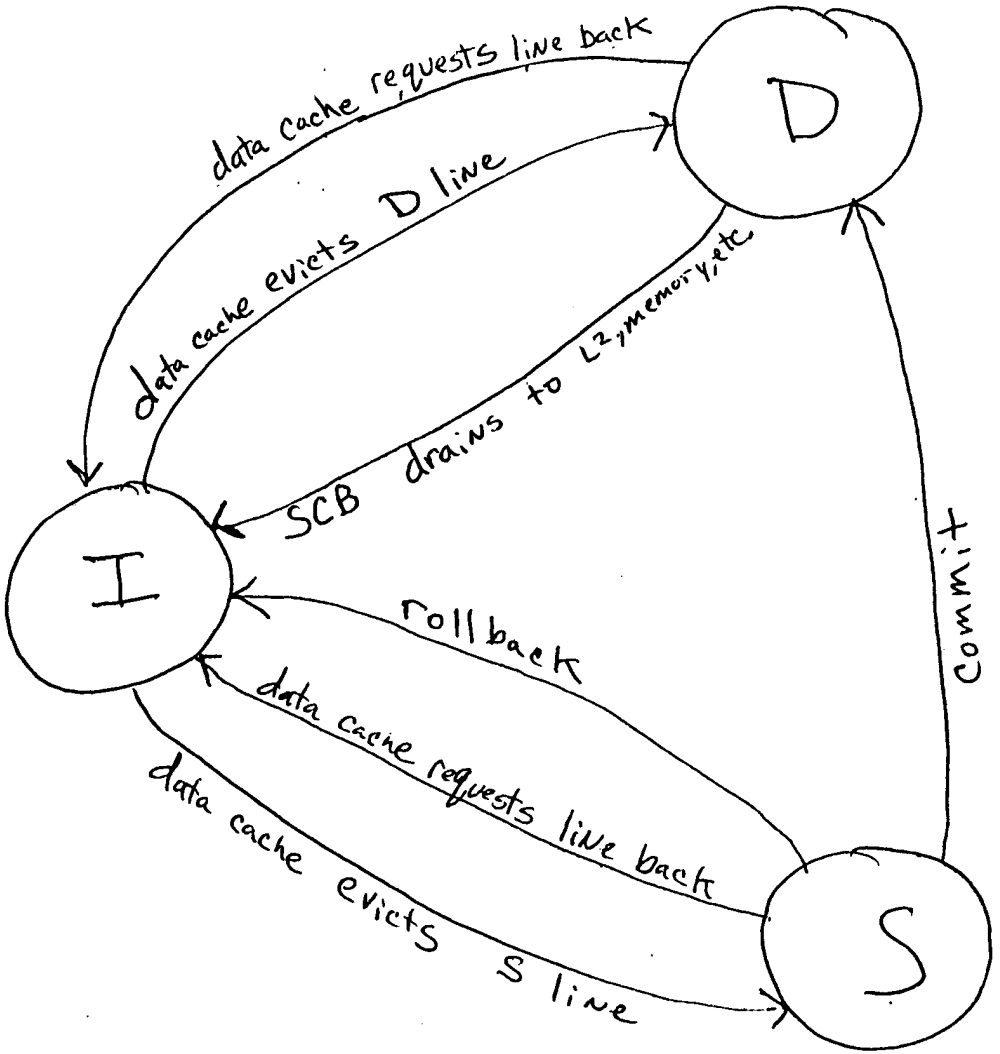
D
I
S
data cache requests line back
data cache evicts D line
SCB drains to L2, memory, etc.
commit
rollback
data cache requests line back
data cache evicts S line

Figure 4

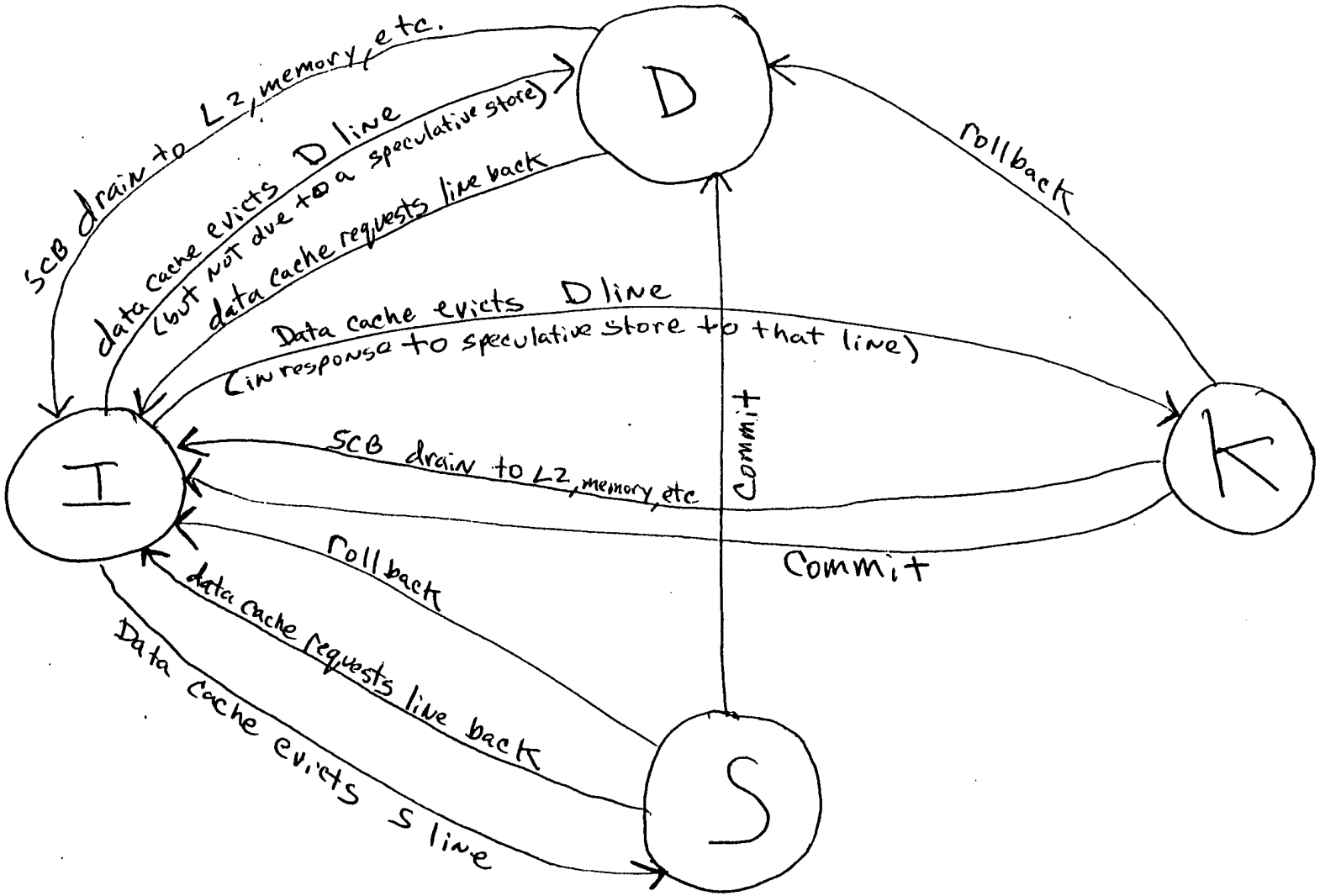
D
I
K
S
SCB drain to L2, memory, etc.
data cache evicts D line
(but NOT due to a speculative store)
data cache requests line back
Data cache evicts D line
(in response to speculative store to that line)
rollback
SCB drain to L2, memory, etc
Commit
Commit
rollback
data cache requests line back
Data cache evicts S line

Figure 5